**Face-To-Face Student/Supervisor Meeting Record**

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| **Project Title:** | Design and Implementation of a Multi-core Processor using FPGA | **Photo:** |  |
| **Student Name:** | Matteo Bovino | **Student ID:** | 8671055 |
| **Supervisor:** | Dr Server Kasap | **Student UID:** |  |
| **Supervisor UID:** |  | **Department:** | AAEEE |
| **Course Code:** | Electrical and Electronic Engineering | **Module Code:** | 306AAE |
| **Date Today:** | 19/03/2021 | **Time:** | 02:00 PM |

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| **Current Progress and Issues:** | |
| *In this meeting we discussed about the issues encountered during the synthesis and implementation of the code. Many problems arose when the design was synthesized in Vivado. Timing and physical constraints alongside the high number of inferred latches caused multiple warmings and errors. Some of these problems could be solved quite rapidly after a simple code review, while others, like skew and latches, proved to be more complex and time consuming.* | |
| **Agreed Key Action Points:** | |
| *After reviewing some of the issues in the synthesized design, we have agreed to set a virtual deadline for the actual implementation of the system. In the upcoming two weeks, I will have to obtain a correct synthesized design that can be implemented in the Nexys 4DDR board. After this period, the dissertation and presentation phase of the project must begin, this is the time in which I will solely focus on the report and no longer make any design changes. I hope to meet the deadline and program the board correctly, however, if I fail to do so, the overall project won’t be impacted due to the new regulations surrounding the final year project.* | |
| **Date and Time of next meeting:** | 02:00 PM 02/04/2021 |

*Signatures of those present:*

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| **Supervisor:** |  |
| **Student: Matteo Bovino** |  |